ABSTRACT OF THE DISCLOSURE

According to one aspect of the present invention, a semiconductor memory device has: a semiconductor layer formed on an insulating film; and a memory cell array including a matrix arrangement of a plurality of memory cells each made up of first and second transistors connected in series, one side of each memory cell being connected to a bit line and the other side of each memory cell being supplied with a reference potential, and according to another aspect of the present invention, a semiconductor memory device manufacturing method includes : forming an oxide layer and a silicon active layer on a semiconductor substrate; forming an element isolation region for separating said silicon active layer into discrete element-forming regions to be substantially flush with said silicon active layer; forming gate electrode of paired two transistors by depositing a gate electrode material on said silicon active layer and patterning it; injecting predetermined ions into a region for forming a diffusion layer in, using said gate electrodes as an ion injection mask; forming said paired transistors by activating the injected ions through a heat process; and forming a first gate line connected to the gate electrode of one of said paired transistors and a second gate line connected to the gate electrode of the other of said paired transistors.